F00 E21 Lab Lecture #1

Parity: simple error-detection

Error detection: use a dictionary of code words that is a subset of the 2^n possible code words

- A failure occurs when an invalid code word is sent

Say we want to know all cases where a single bit might be flipped

- Think about a hypercube, where each node represents a bit string
- Each node only takes a one bit modification to get to its neighbor
- Distance is defined as how many steps you have to take to get between two nodes

If we want to know when any single bit is flipped, which nodes on the hypercube can we use?

- Any set of nodes such that no two valid code words are less than a distance 2 apart
- using a parity bit (either even or odd parity) allows such a code

Designing a simple digital circuit

Process:

1. Problem description
2. Truth Table
3. Karnaugh Map
4. Boolean Equation
5. Logic Circuit Diagram

Problem description:

Design a half-adder (2 inputs (A, B), 2 outputs (Sum, Carry)

Design a full-adders (3 inputs (A, B, CarryIn), 2 outputs (Sum, Carryout)

Truth Table:

Carry In	A	B	Sum	Carry Out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Karnaugh Map

A Karnaugh map is a way to generate a circuit description from a truth table

- Arrange the inputs along the axes
- The output value for a set of inputs appears in the appropriate box
- Circle adjacent sets with size 2^n
- Each set forms a product term
- The final circuit is a sum (OR) of products (AND)

Table 1: Karnaugh Map for Full-adder Sum term

Sum Output	CA = 00	CA = 01	CA = 11	CA = 10
B = 0	0	1	0	1
B = 1	1	0	1	0

Table 2: Karnaugh Map for Full-adder Carry term

Carry Out-put	CA = 00	CA = 01	CA = 11	CA = 10
B = 0	0	0	1	0
B = 1	0	1	1	1

Equation

Write the sum of each term from the Karnaugh Map

Sum = $\overline{CA}B + \overline{C}A\overline{B} + CAB + C\overline{AB}$

Carry Out = AB + CB + AC

Logic Diagram

Write a logic circuit implementation the equation (Sum of Product terms)

- Each product of N-input terms is an N-input AND gate
- The product terms are connected by OR gates